# Laboratory Report # 2

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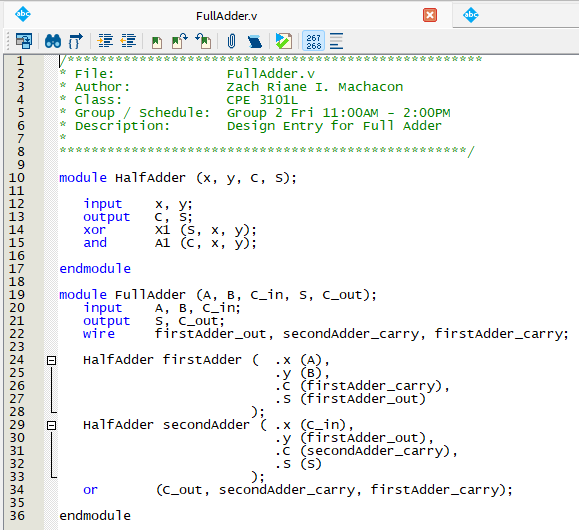
**Laboratory Exercise Title:** Basic Constructs in Verilog HDL

***Target Course Outcomes:***

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

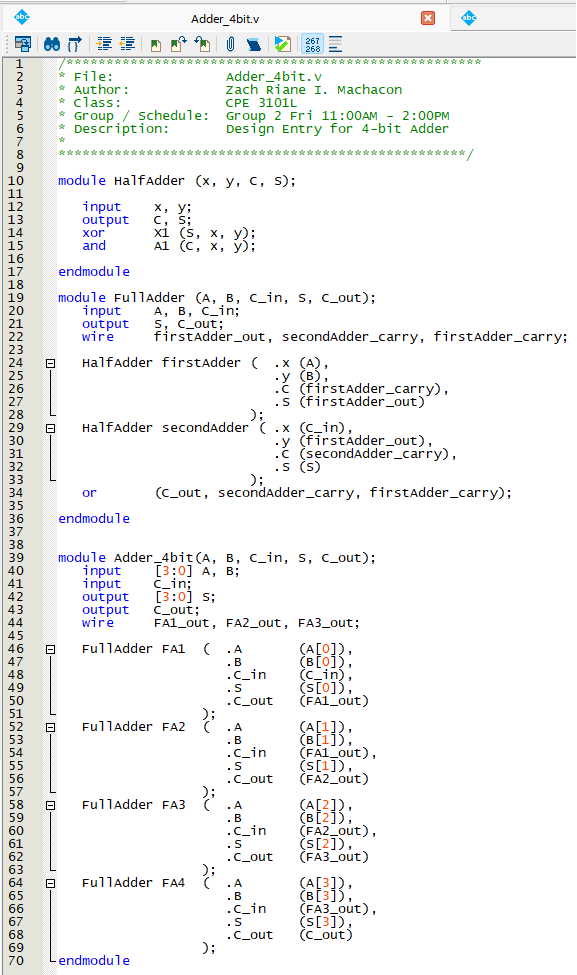
**CO2:** Verify the functionality of HDL-based components through design verification tools.

**Exercise 2C:**



**Figure 1: Design Entry for FullAdder in Verilog HDL**

The FullAdder module makes use of structural modeling where it instantiates 2 HalfAdders to create a Full Adder. An OR gate primitive is also used to get the final carry out.

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**Figure 2: Design Entry for 4-bit FullAdder in Verilog HDL**

The Adder\_4bit module also utilizes structural modeling. Building off the previous FullAdder and HalfAdder modules, the Adder\_4bit module instantiates 4 FullAdders to create the 4-bit Full Adder.

A screenshot of a computer

Description automatically generated

**Figure 3: Compilation Report for the Flow Summary of Adder\_4bit**

According to the compilation report, 8 logic elements and 14 total pins are needed. Quartus also found 1 warning, however, it is negligible and does not interfere with the synthesis process.

A computer screen shot of a diagram

Description automatically generated

**Figure 4: Schematic Diagram of Synthesized Circuit from Adder\_4bit Project**

To create the 4-bit Full Adder, 4 Full Adders are connected in sequence with each next adder’s carry-in being the previous adder’s carry-out. Each sum calculated from the Full Adders contribute the final 4-bit sum while the final carry-out is the carry-out of the final adder.

A screenshot of a computer

Description automatically generated

**Figure 5: Verilog Testbench File for Adder\_4bit Project**

The testbench files contain several test inputs which are in decimal. This is to ensure that the 4-bit Full Adder is outputting the correct answers.

A computer screen shot of a black screen

Description automatically generated

A B C\_in

-1 + -1 + 1

C S

= 0 -1

A B C\_in

-1 + -1 + 0

C S

= 0 -2

A B C\_in

1 + -7 + 0

C S

= 0 -6

A B C\_in

5 + 4 + 1

C S

= 0 -6

A B C\_in

-4 + 6 + 0

C S

= 0 2

A B C\_in

-5 + 3 + 0

C S

= 0 -2

A B C\_in

3 + -8 + 1

C S

= 0 -4

A B C\_in

0 + 0 + 0

C S

= 0 0

**Figure 6: Verilog Testbench Waveform for Adder\_4bit Project**